

Fig. 1

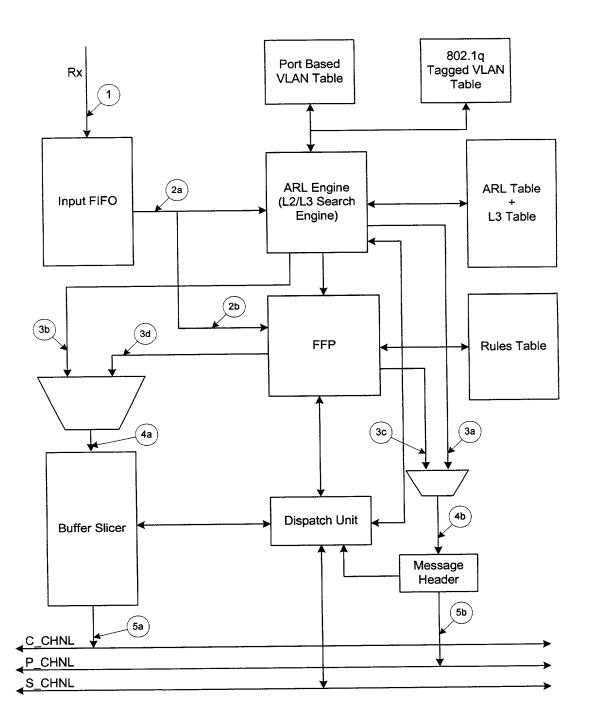


Fig. 2

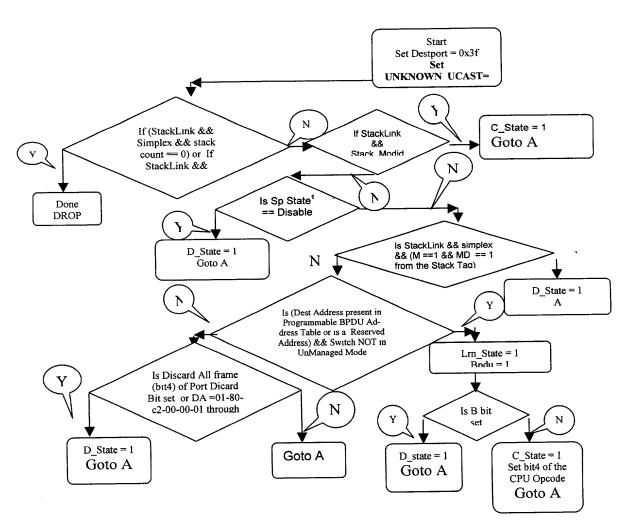


Fig. 3

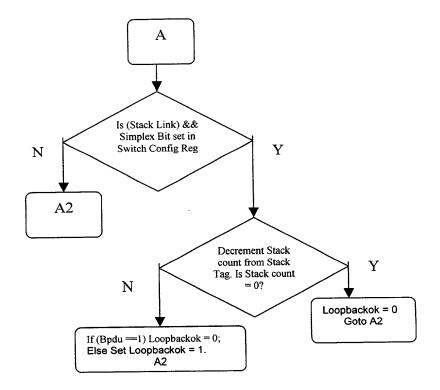


Fig. 4

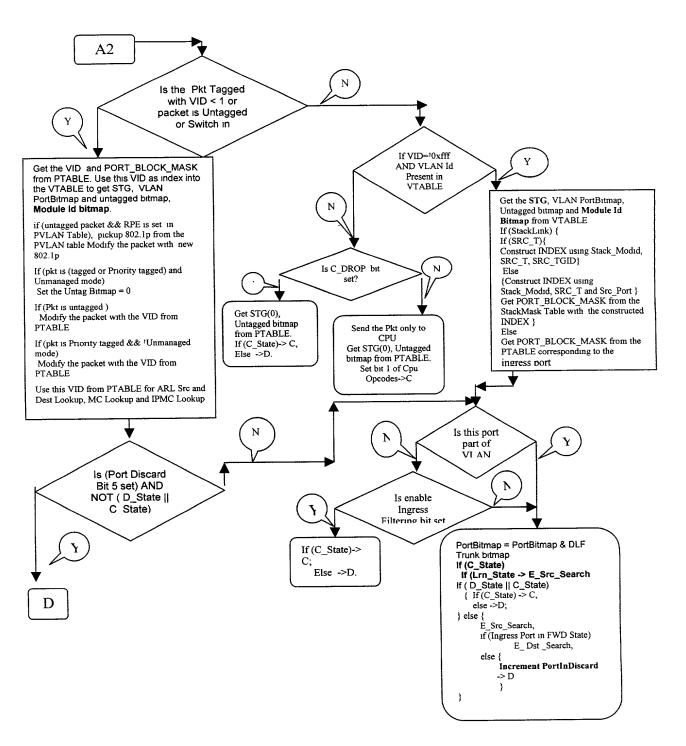


Fig. 5

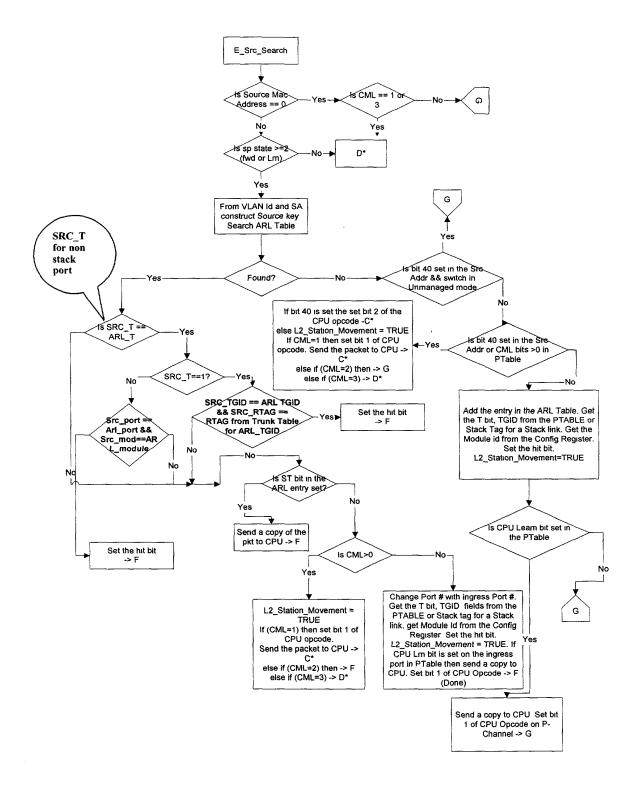


Fig. 6

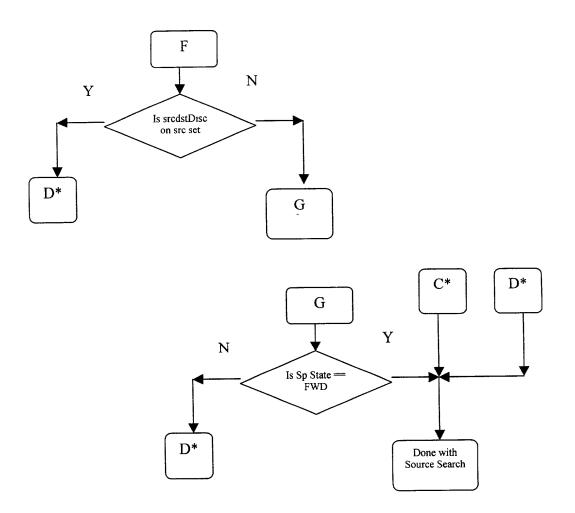


Fig. 7

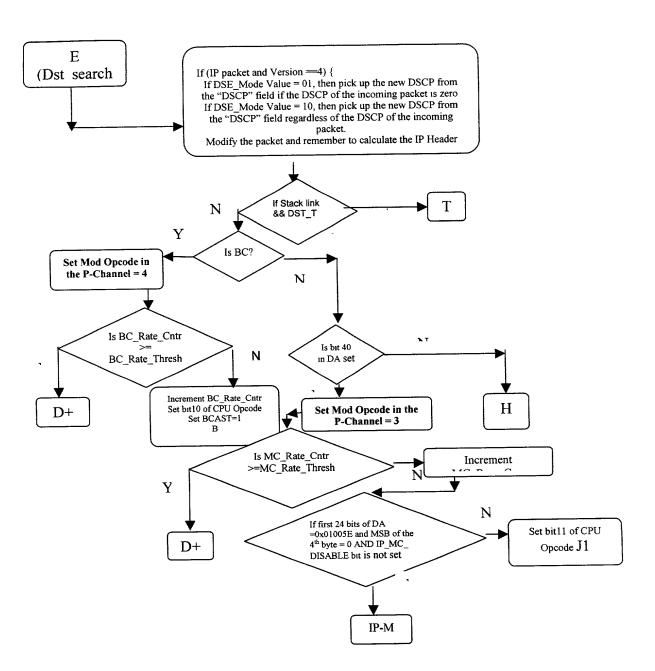


Fig. 8

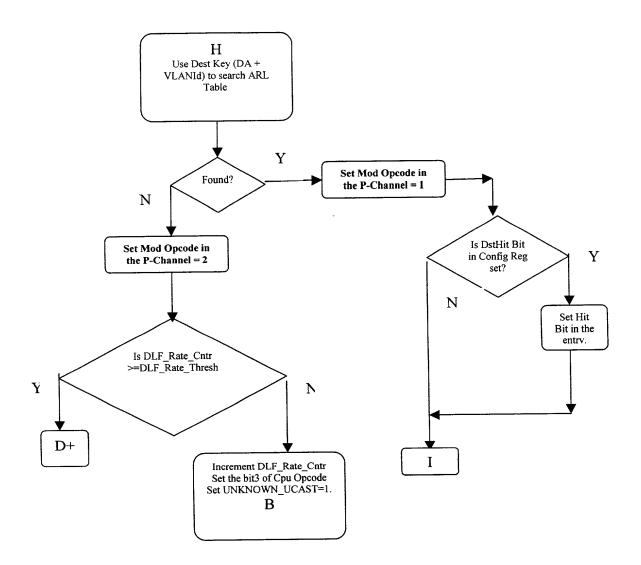


Fig. 9

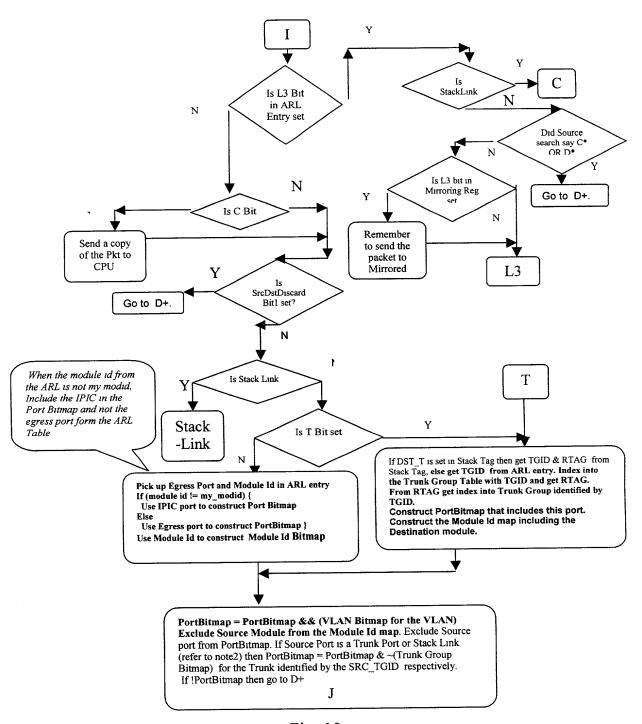


Fig. 10

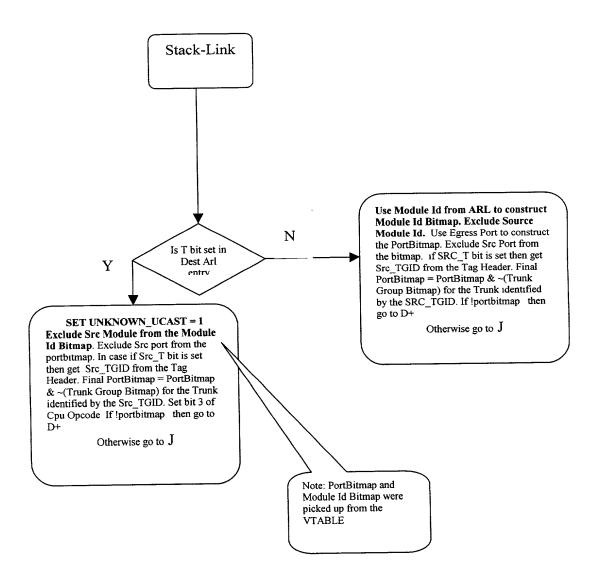
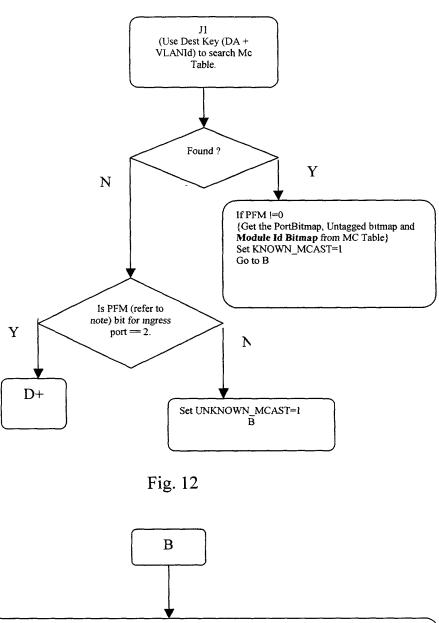


Fig. 11



Exclude Source Module from the Module Id map. Exclude Source Port from the portbitmap. If the Source Port is a Trunk Port or Stack Link (refer to note 2) then Final Bitmap = egress portbitmap & ~(Trunk Group Bitmap)

If |PortBitmap then go to D+ ->

J

Fig. 13

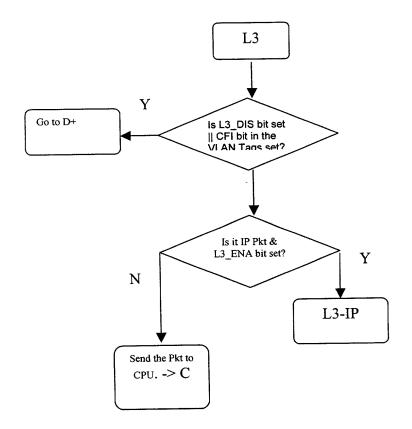


Fig. 14

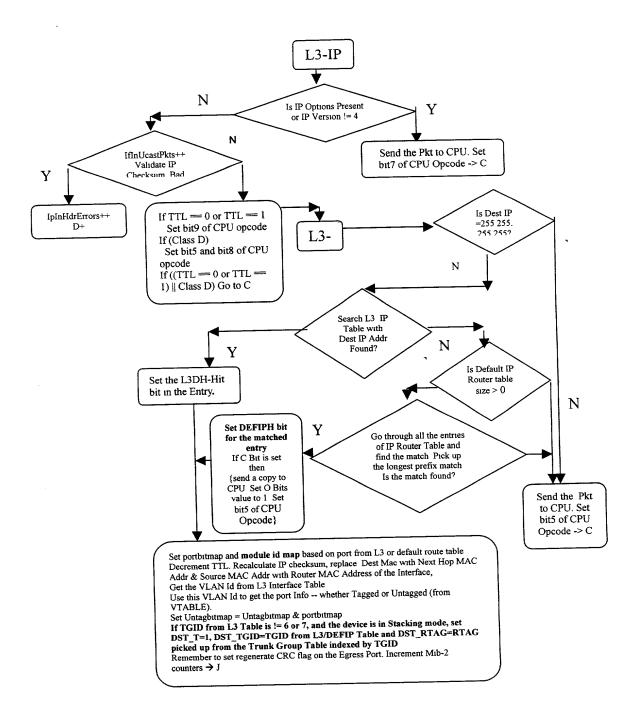


Fig. 15

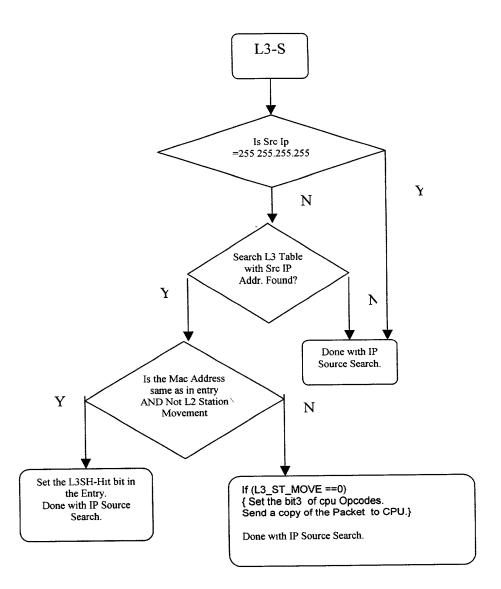


Fig. 16

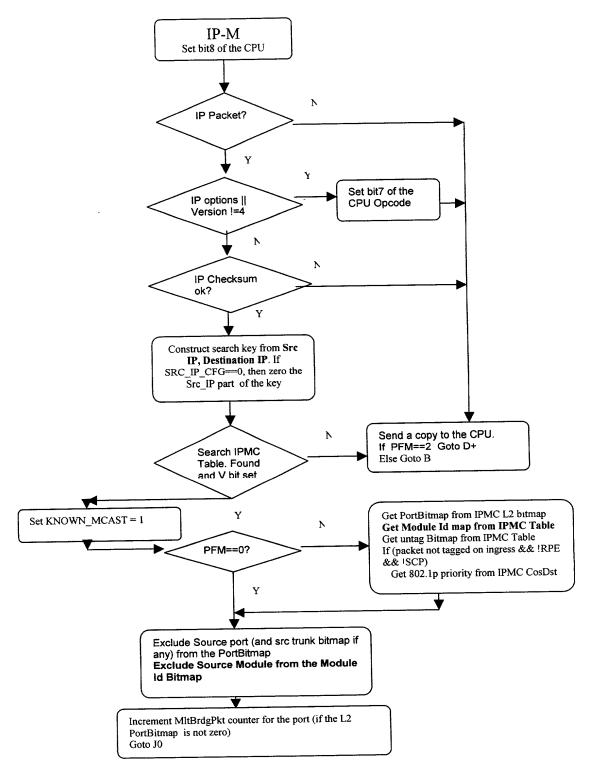


Fig. 17

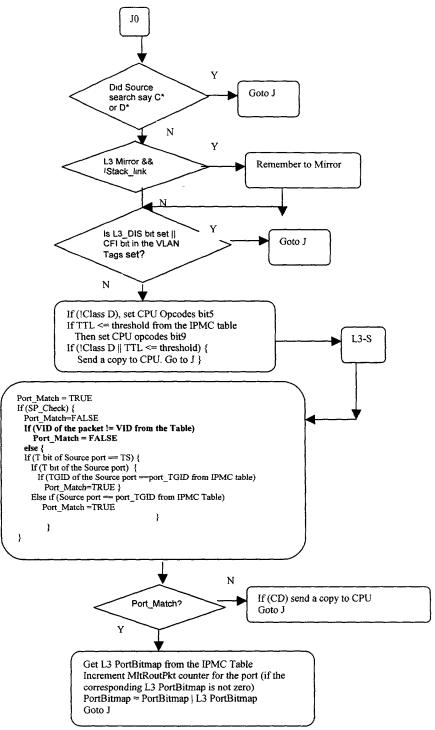


Fig. 18

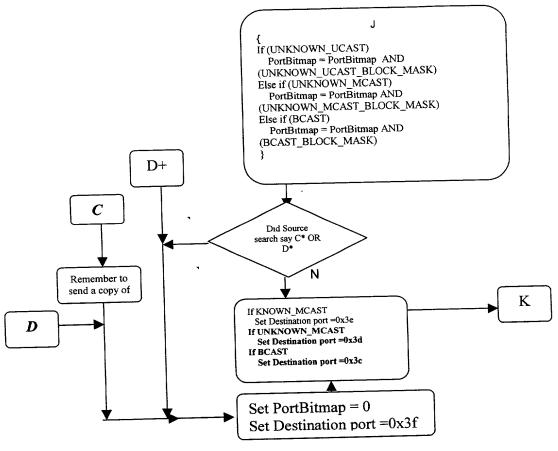


Fig. 19

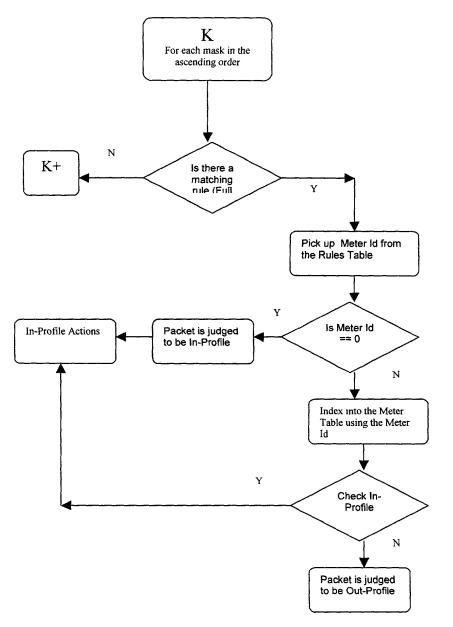


Fig. 20

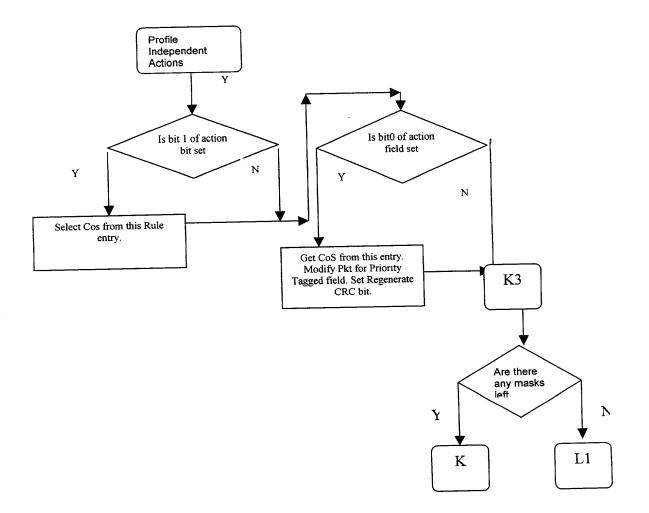


Fig. 21

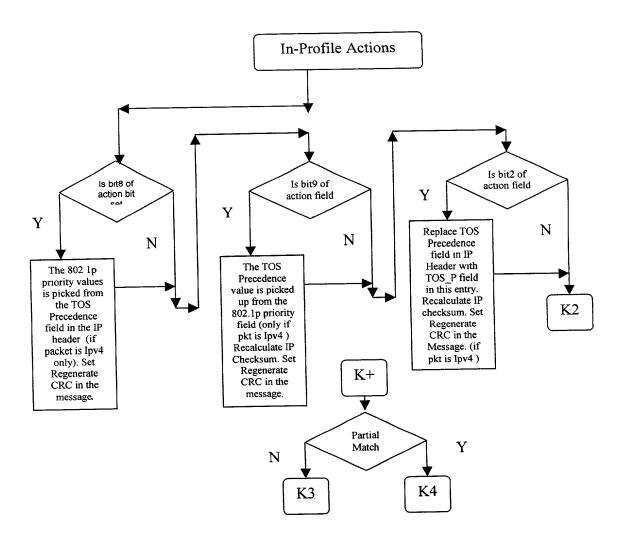
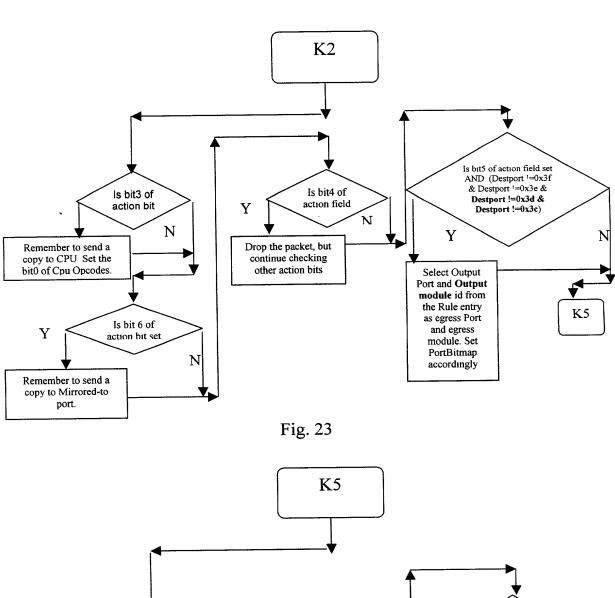


Fig. 22



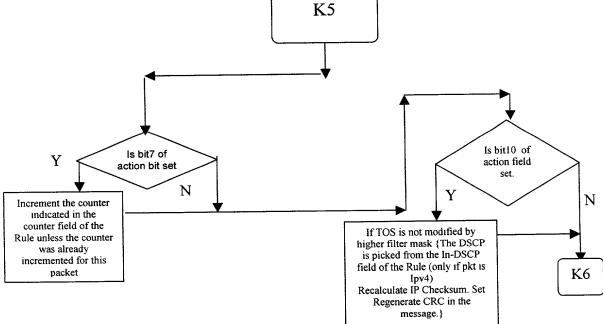


Fig. 24

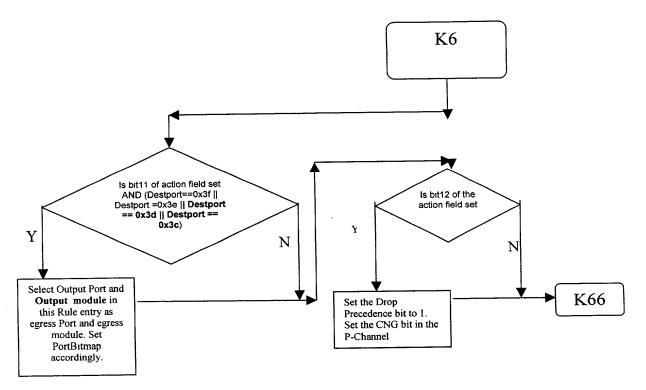


Fig. 25

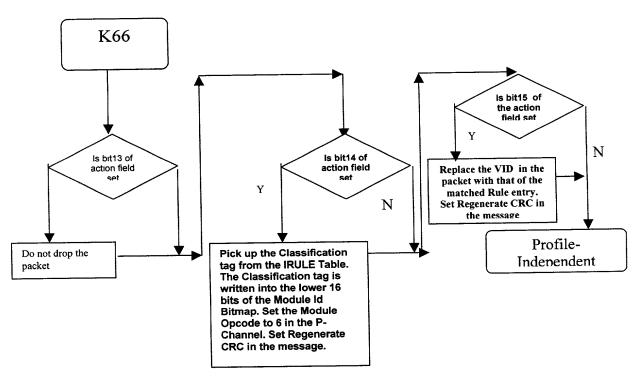


Fig. 26

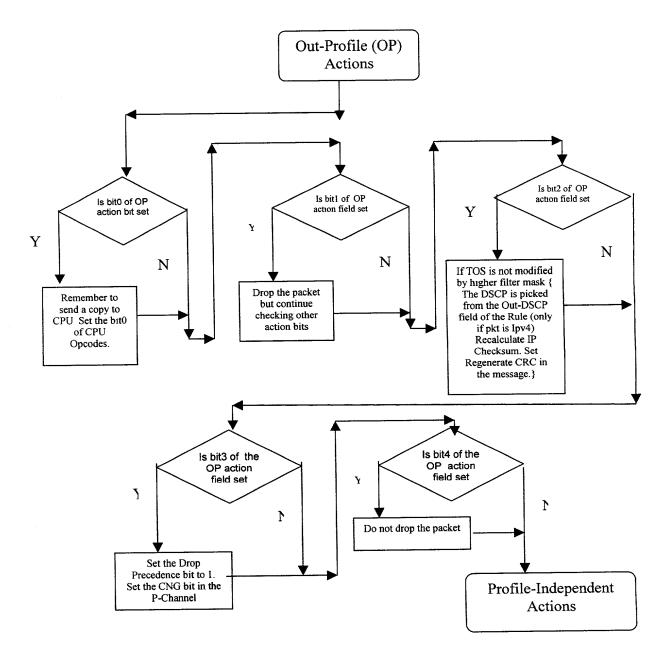


Fig. 27

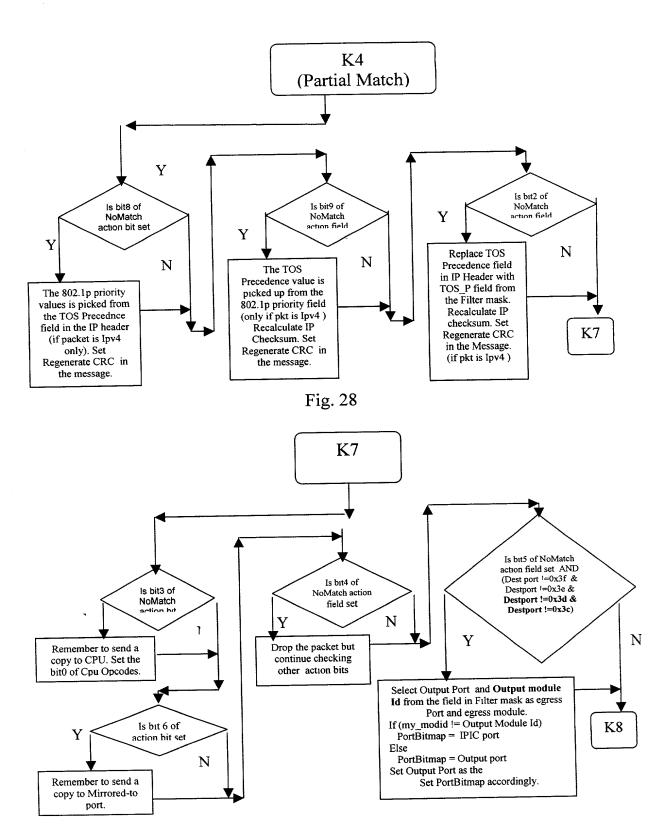


Fig. 29

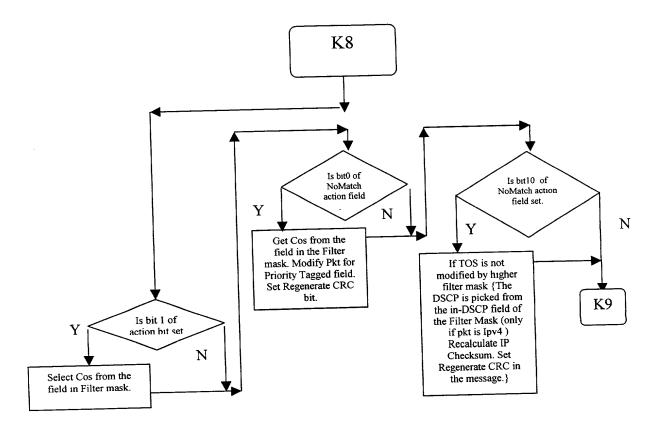


Fig. 30

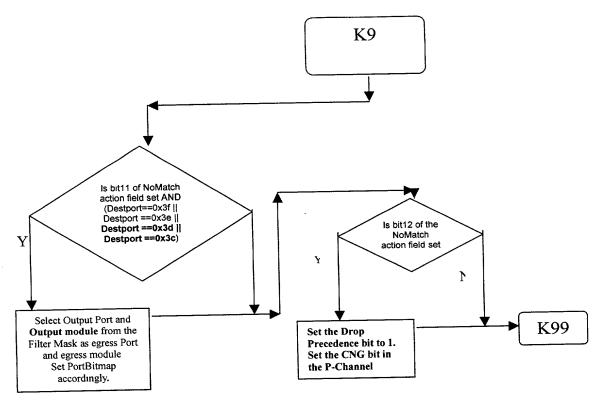


Fig. 31

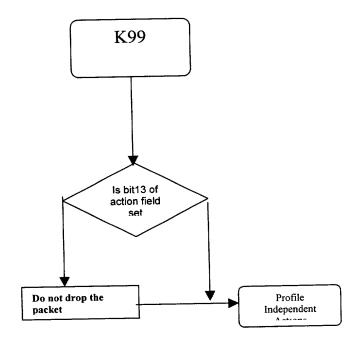


Fig. 32

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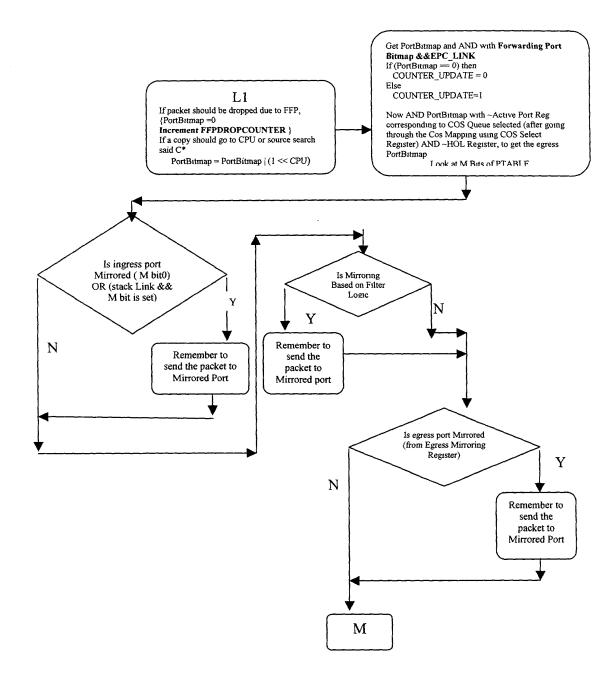


Fig. 33

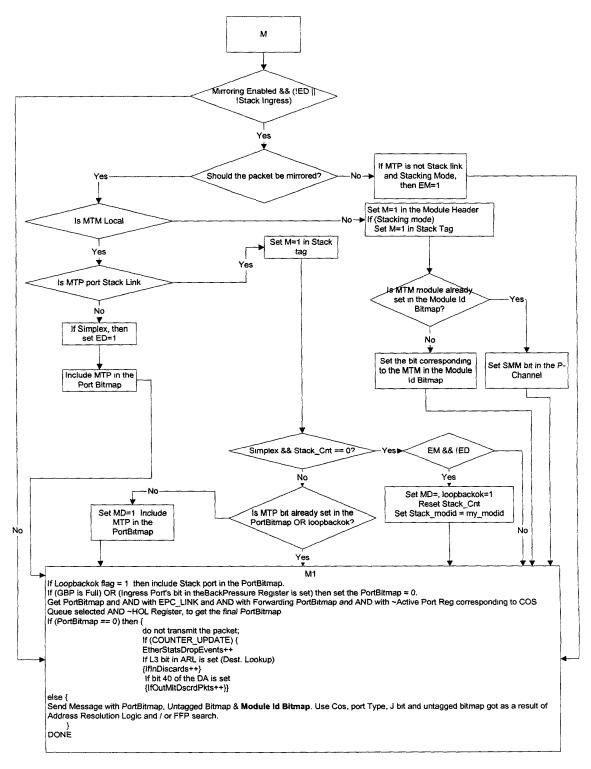


Fig. 34

1 - C - A

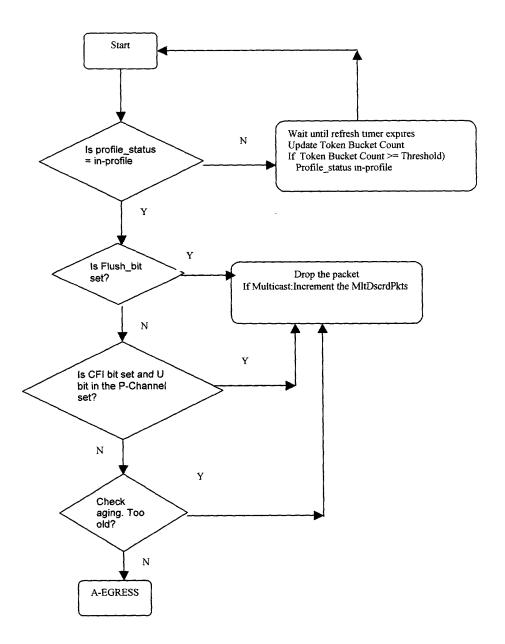


Fig. 35

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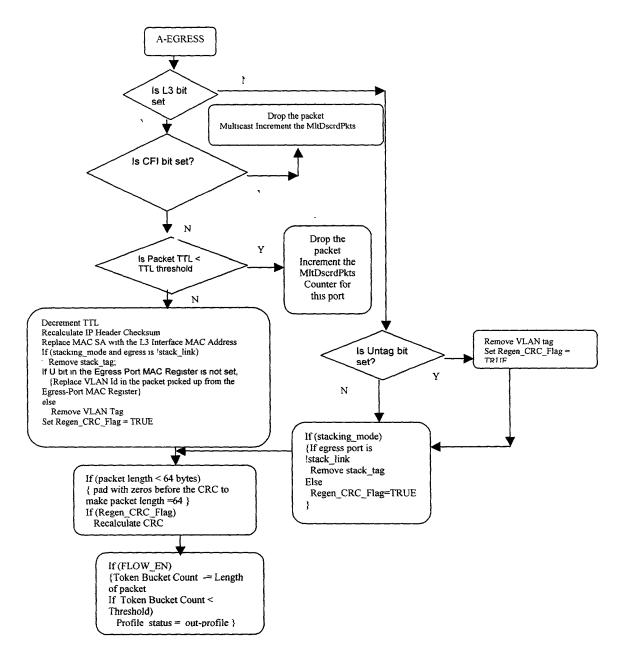


Fig. 36

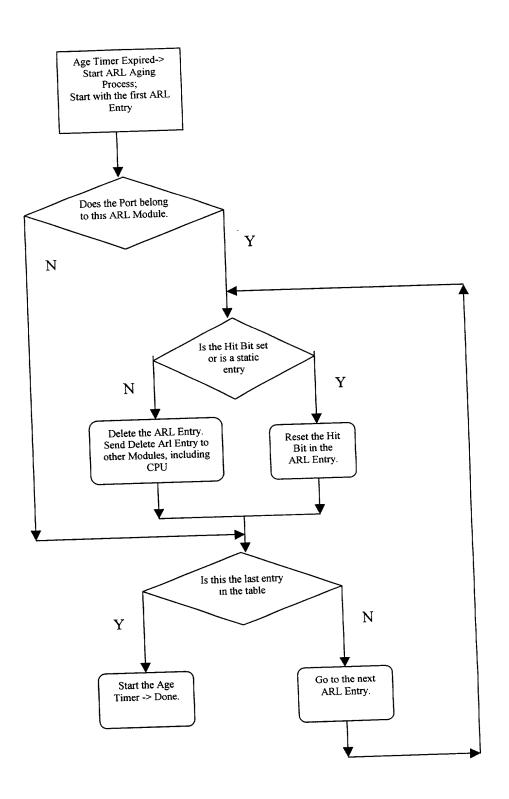
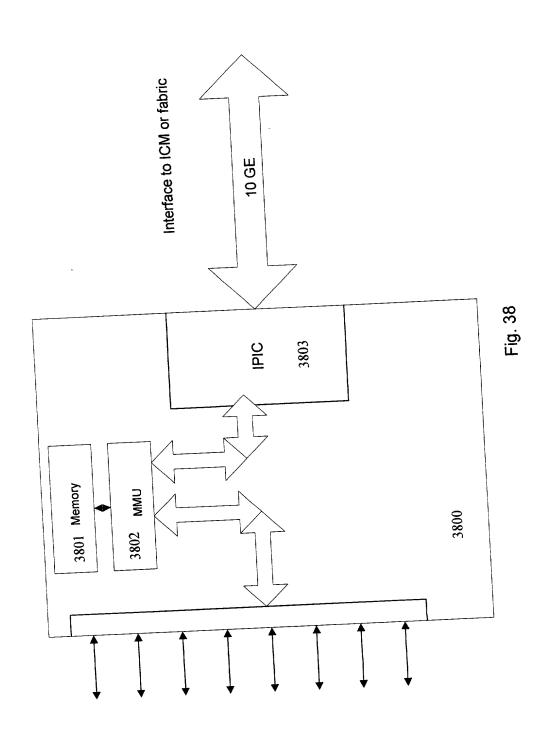


Fig. 37



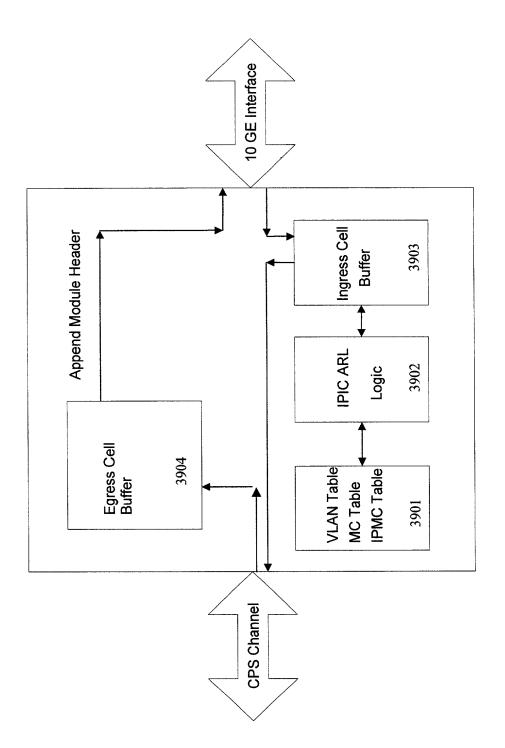


Fig. 39

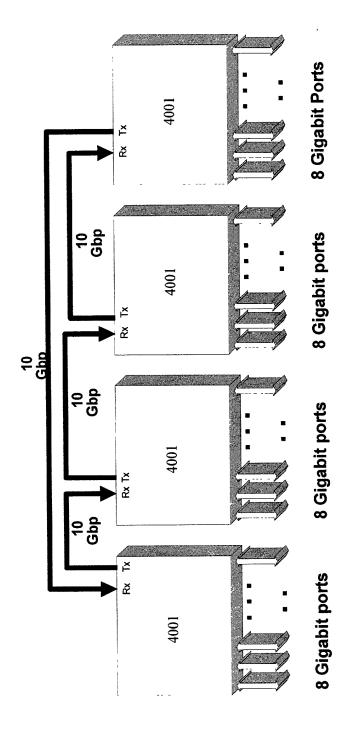
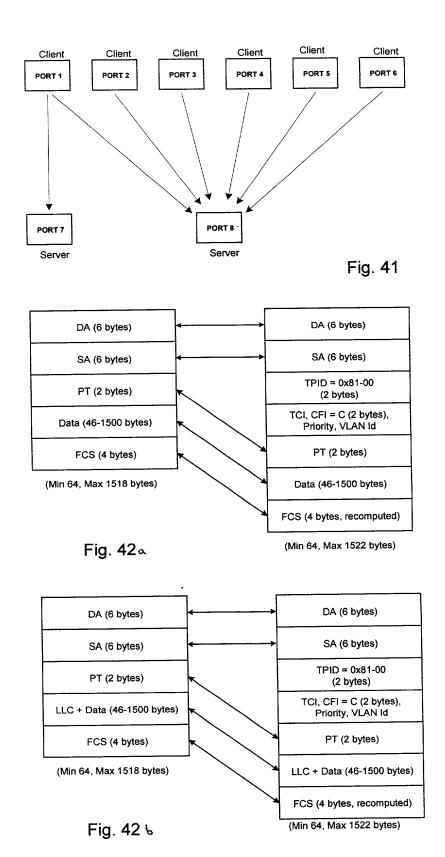


Fig. 40



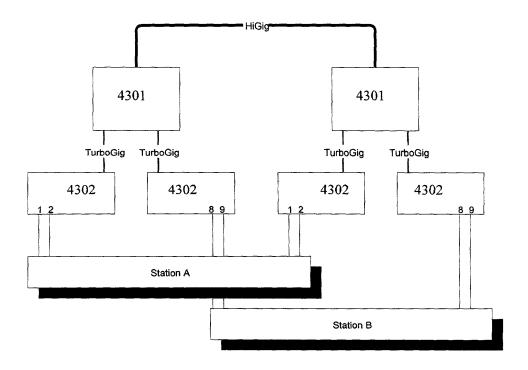


Fig. 43

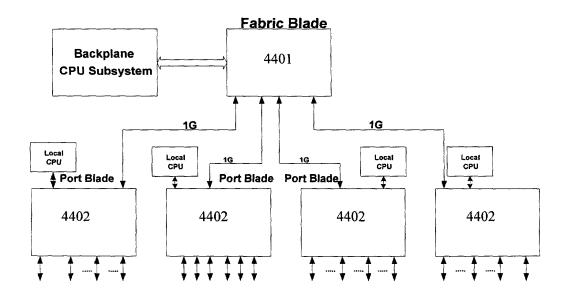


Fig. 44

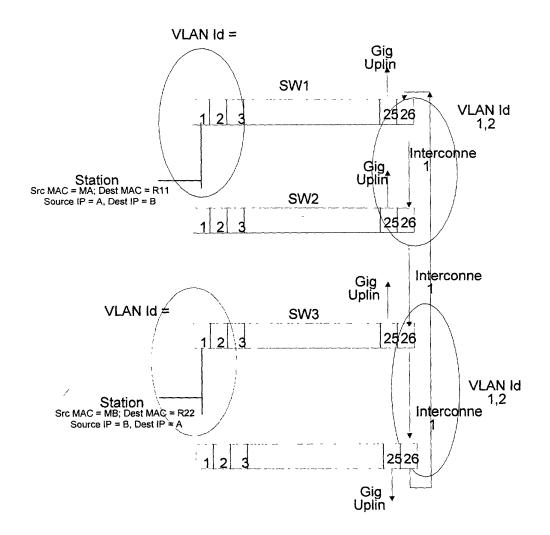


Fig. 45

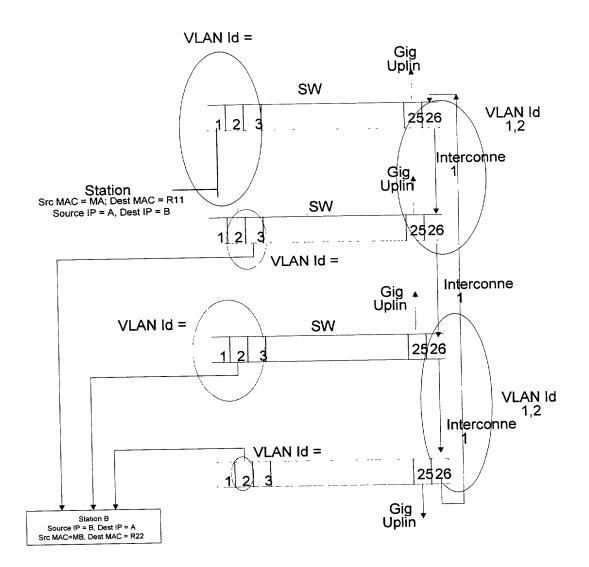


Fig. 46